NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

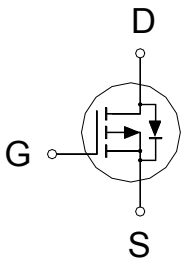
P4404EDG

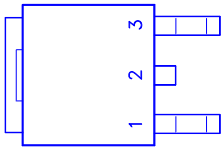
TO-252(DPAK)

Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	44mΩ	-20A





1. GATE
2. DRAIN
3. SOURCE

100% Rg tested

100% UIS tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	-20	A
	T_C = 70 °C		-16	
Pulsed Drain Current[1]		I_{DM}	-50	
Avalanche Current		I_{AS}	-18	
Avalanche Energy [2]	L = 0.3mH	E_{AS}	48	mJ
Power Dissipation	T_C = 25 °C	P_D	30	W
	T_C = 70 °C		19	
Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		4.1	°C / W
Junction-to-Ambient	$R_{\theta JA}$		80	°C / W

[1]Pulse width limited by maximum junction temperature.
[2]V_{DD} = -20V . Starting T_J = 25°C.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.7	-1.9	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -32V, V_{GS} = 0V			1	μA
		V_{DS} = -30V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-50			A

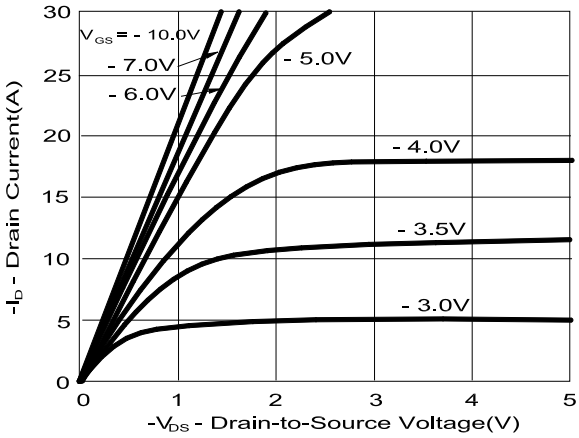
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -8A		57	68	mΩ
		V_{GS} = -10V, I_D = -10A		38	44	
Forward Transconductance[1]	g_{fs}	V_{DS} = -10V, I_D = -10A		11		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -20V, f = 1MHz		850		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge[2]	Q_g	V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = -10V, I_D = -10A		14		nC
Gate-Source Charge[2]	Q_{gs}			2.2		
Gate-Drain Charge[2]	Q_{gd}			1.9		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		3.5	5	Ω
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -20V, R_L = 1Ω, $I_D \cong$ -1A, V_{GS} = -10V, R_{GS} = 6Ω		6.0	12.8	nS
Rise Time[2]	t_r			9.2	18.6	
Turn-Off Delay Time[2]	$t_{d(off)}$			19.2	34.8	
Fall Time[2]	t_f			11.8	21.6	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-20	A
Forward Voltage[1]	V_{SD}	I_F = -10A, V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -5 A, dI_F/dt = 100A / μS		15.5		nS
Reverse Recovery Charge	Q_{rr}			7.9		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

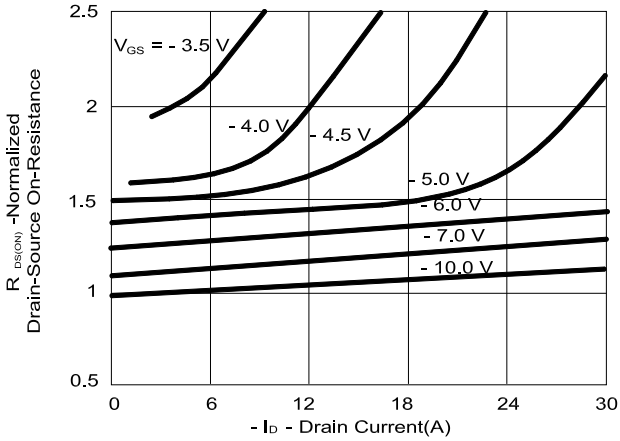
REMARK: THE PRODUCT MARKED WITH "P4404EDG", DATE CODE or LOT #

TYPICAL PERFORMANCE CHARACTERISTICS

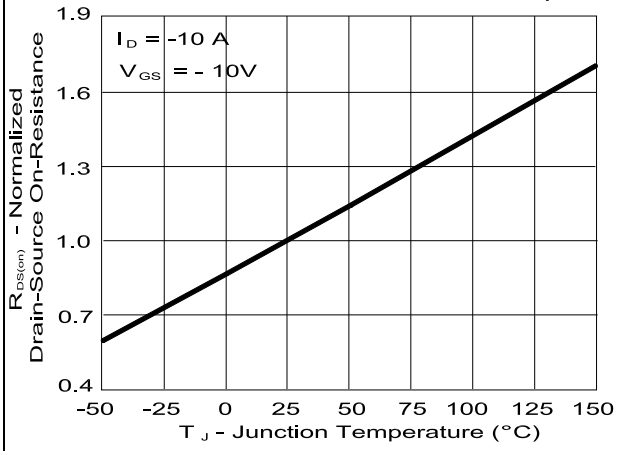
On-Region Characteristics



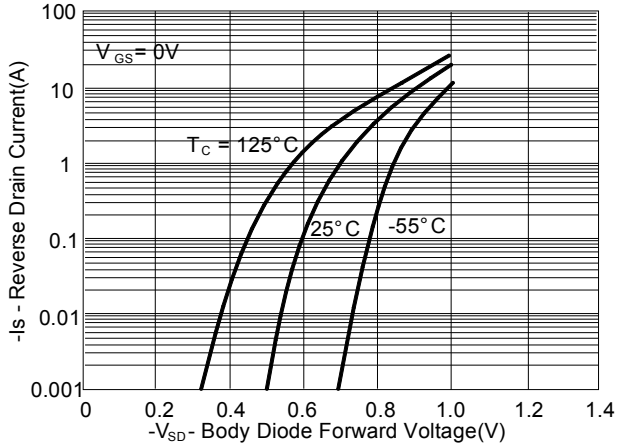
On-Resistance Variation with Drain Current and Gate Voltage



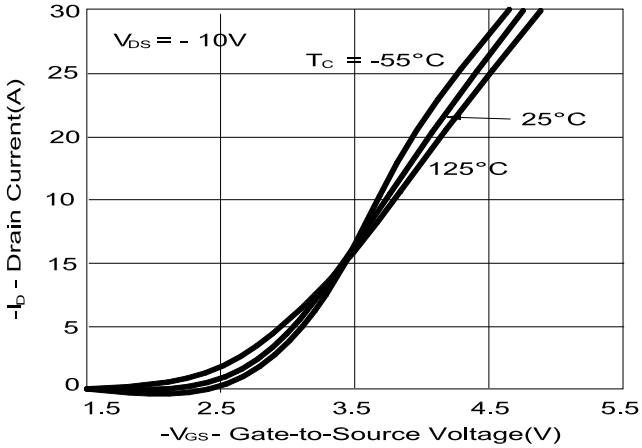
On-Resistance Variation with Temperature



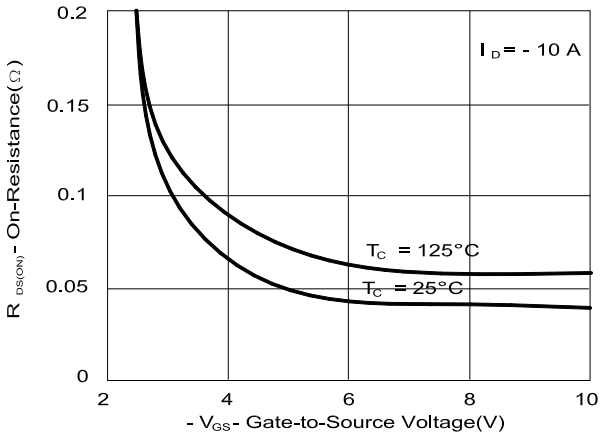
Body Diode Forward Voltage V.S Source Current



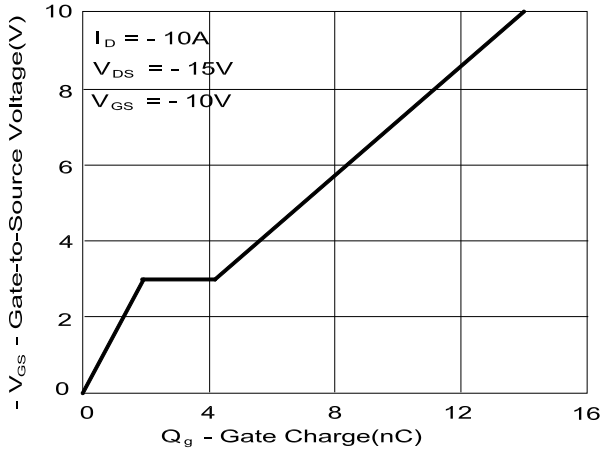
Transfer Characteristics



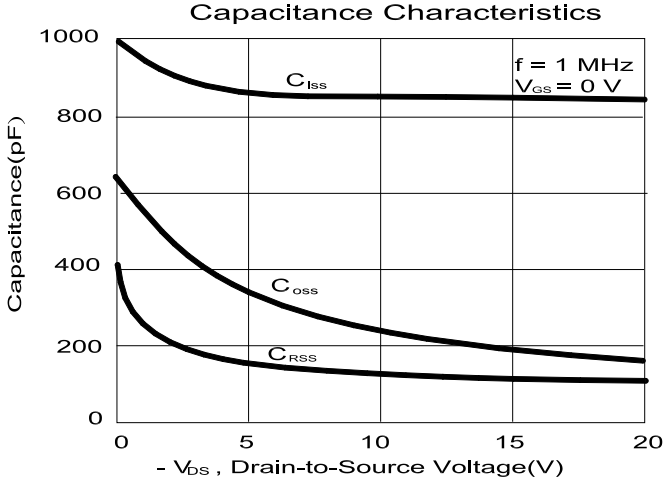
On-Resistance Variation with Gate-to-Source Voltage



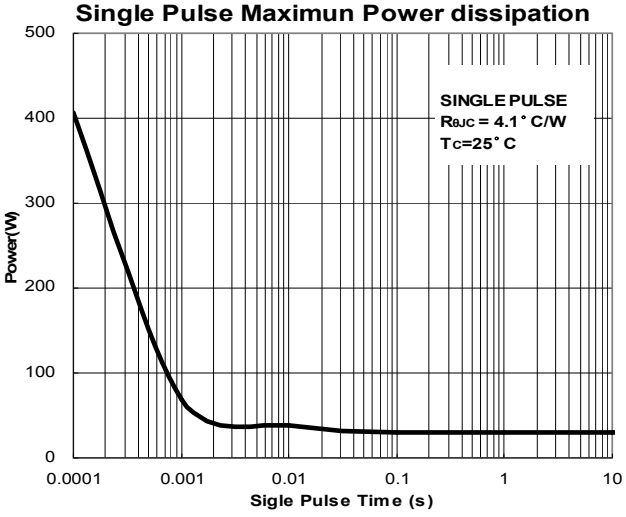
Gate Charge Characteristics



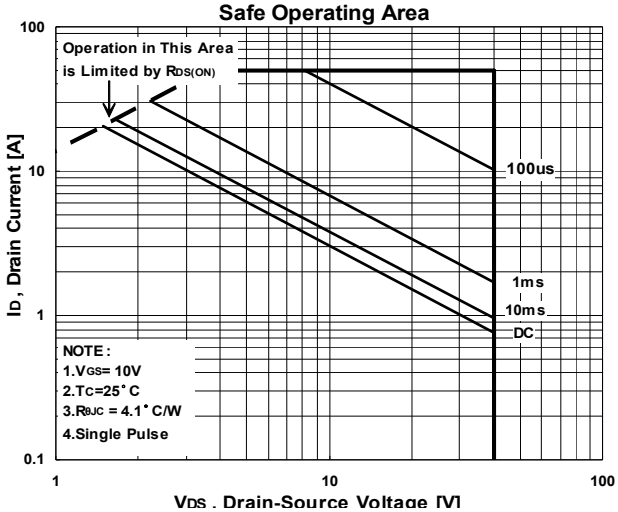
Capacitance Characteristics



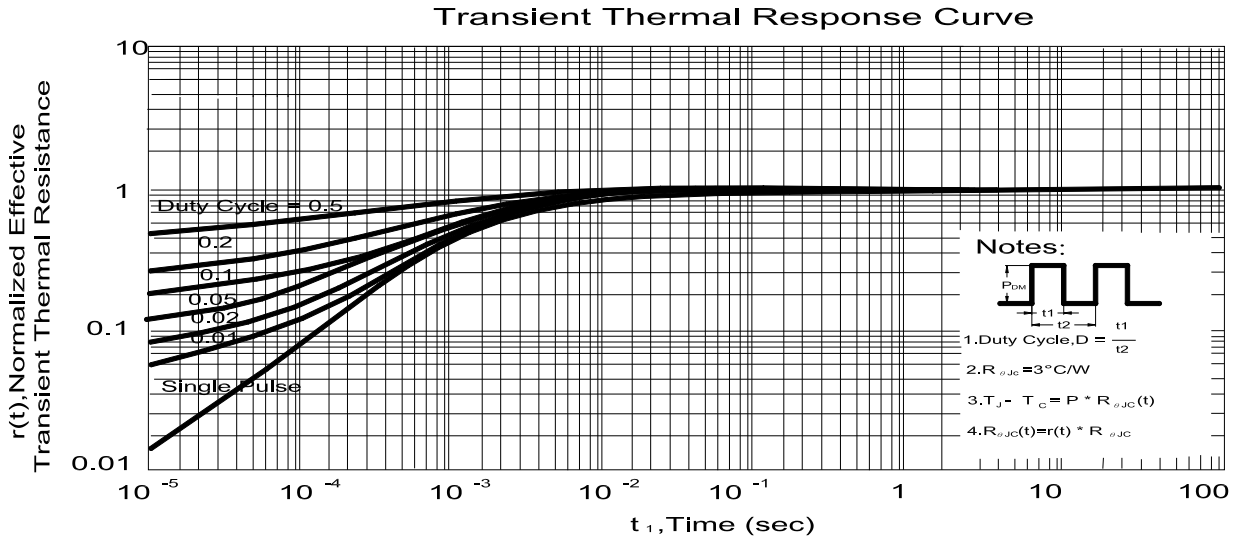
Single Pulse Maximun Power dissipation



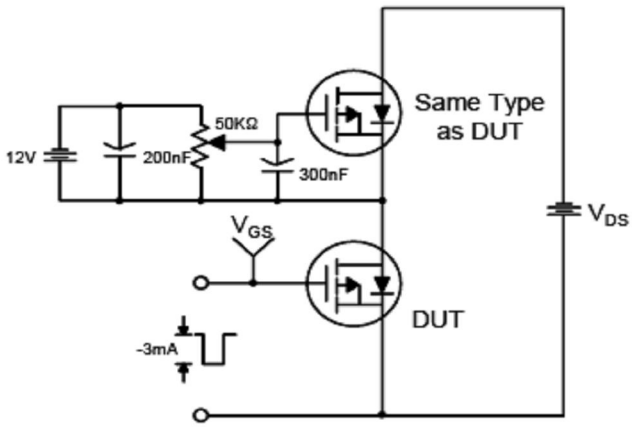
Safe Operating Area

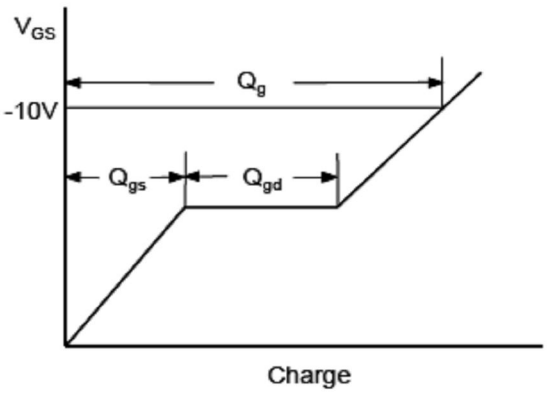


Transient Thermal Response Curve

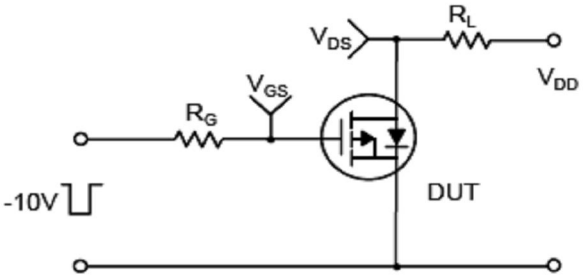


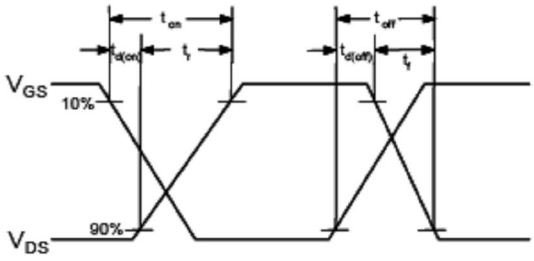
Gate Charge Test Circuit & Waveform



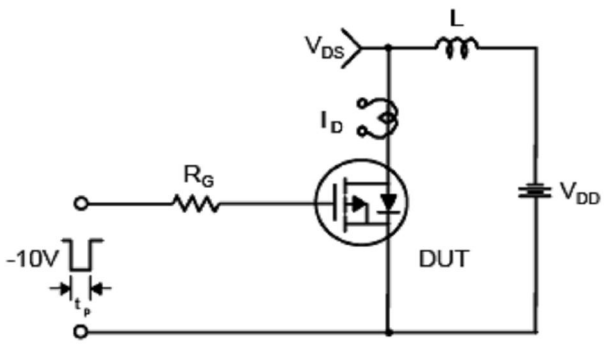


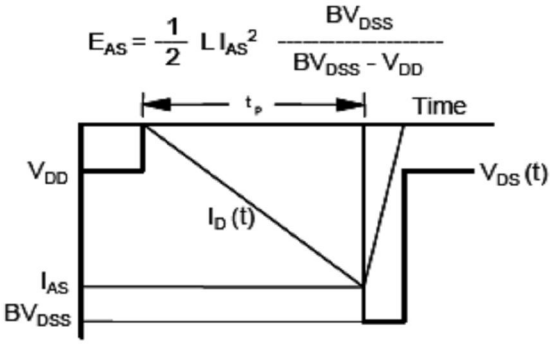
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching Test Circuit & Waveforms





Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	9.5	10.4	H	0.8	1.27	2.03
B	2.19	2.3	2.435	I	6.35	6.6	6.8
C	0.35	0.5	0.65	J	4.8	5.34	5.5
D	0.89		1.5	K	0.5		1.5
E	0.35		0.65	L	0.4	0.76	0.89
F	0.0		0.23	M	3.96		5.18
G	5.4		6.2	W	3.38	3.58	3.78